FDC-II

User Manual

Addendum to Appendix C

A. Qume DT8

If double sided operation is desired the option labeled "2S" should be jumpered. The "2S" option can be left open if the only requirement is single sided operation.

B. Shugart 800/801/850/851

Page 13 of appendix C should read:

Shugart 800/801

The required drive configuration for the 850/851 models is included as a separate page in appendix C.

C. Mixed size system

If there is a requirement to operate both 8" drives and 5 1/4" drives from the same controller, consideration must be given as to the amount of write precompensation that is needed by each drive. If the 5 1/4" drives require an amount that is other than twice what is required on the 8" drives, a modification to the switching circuit is needed. Contact Teletek Enterprises for further details.

ERRATA
Revision 6 FDC-II Changes
4/24/81

Pre-Write Compensation

The pads PW, FD, and NC on the back of FDC-II have been replaced by three posts and a shorting plug located above IC 8A on the front of FDC-II. The left post is PW, the center is FD, and the right post is NC.

Boot PROM disable

The disable jumper pads on the back of FDC-II have been replaced by two posts and a shorting plug located below capacitor C18 on the front of FDC-II. If the plug is inserted the boot PROM is enabled and if removed the PROM is disabled.

DC/jd
rev. 4/24/81

Revision 6, March 1980

Table of Contents

I/O and memory addressing are jumper selectable. Normally, the 1k data buffer on the FDC-II is addressed for F400 to F7FFH addresses. The standard operating systems and the boot strap PROM provided with the FDC-II assume standard addressing. The port addresses for FDC-II are normally set to 60H through 7FH.

The disk drive interface is ANSI standard. This means that any ANSI-compatible disk drive can plug directly into the FDC-II.

Any IEEE-100 compatible CPU can be used with the FDC-II, regardless of clock speed, but the boot software in the on-board PROM and the standard operating system available from Teletek are only 8080/Z80 compatible. Some of the operating systems which will function with the FDC-II are CP/M and OASIS.

Note: More than one FDC-II can be in a system at the same time. The only requirement is that the port and data buffer addresses do not conflict.

Installation

Visual Inspection

Upon receipt of the FDC-II, carefully inspect for any damage which may have occurred during shipping. Check that all IC's are firmly in their sockets and that nothing is broken. If you have ordered an operating system with the FDC-II, check that the diskette provided has not been damaged. Diskettes can be damaged by bending them or by exerting undue pressure which warps the surface of the diskette.

Jumper Selection

The standard FDC-II comes equipped with pre-write compensation set for 250 ns, the boot function enabled, the data buffer addressed at F400H, the data buffer enabled, the I/O port address set for 60H, and the mini/maxi boot function jumpered for 8-inch flexible disk drive operation. If any of these functions need to be changed, make the appropriate changes as outlined in the section entitled "Options".

Drive Connections

The FDC-II uses ANSI-compatible drive connectors. The functions and their specific pin number are listed in Figure 1, "FDC-II Floppy Drive Connectors". Any 8-inch floppy disk drive which is ANSI-compatible can be connected by means of a 50 conductor ribbon cable and appropriate connectors on each end without further modification. Any ANSI-compatible 5 1/4-inch drive can be connected via 34 conductor cable and connectors to the on-board 34-pin connector.

In the section entitled "Disk Drive Interfacing", we have listed several of the popular drives and also the configuration which works best when coupled with the FDC-II. In general, most flexible disk drives which have adopted the ANSI standards will be configured similarly to the ones listed. It must be kept in mind that the drive motor for head positioning must be enabled for the NEC 765 to function properly. The reason that this must be so is that the NEC 765 continually checks the status of all drives connected to the system. To do so, it continually polls the various drives; therefore, the select lines are never held continuously except during a data transfer. On those drives where the stepper motor is only enabled when the select line is held, the stepper motor will be disabled during those times when the 765 is checking other drives' status.

Using the FDC-II

With a flexible disk drive configured as necessary and connected to FDC-II and with FDC-II in the system, apply power to the system. If the boot function is enabled, a reset will cause the FDC-II to execute a boot strap load function. The door of the drive must be closed on the diskette with an operating system. The boot strap PROM loads the first sector of track 0 into the system beginning at memory location 0 and then executes that routine. That routine then loads the rest of the operating system. With CP/M, the operating system is contained on tracks 0 and 1 and the FDC-II loads the rest of those tracks into the system then transfers execution to the CP/M operating system. With the proper BIOS in the operating system, FDC-II then will be used by the operating system for all of the data handling necessary to and from the flexible disk drive.

On those flexible disk drives which have an LED on the front door to indicate drive selection, this light will glow dimly during normal operation of the FDC-II. This is an indication that the NEC 765 is continually checking the status of the drives. The LED will glow brightly during read and write operations when the drive is selected continuously.

Floppy Drive Connectors

For 8" Drives

Ground Pin #	Signal Pin #	Input - I Output - O	Description
1	2	O	Above track 43
3	4	-	Not used
5	6	-	Not used
7	8	O	Above track 43
9	10	I	Dual sided
11	12	-	Not used
13	14	O	Head 1
15	16	-	Not used
17	18	O	Head load
19	20	I	Index
21	22	I	Ready
23	24	-	Not used
25	26	O	Drive select 0
27	28	O	Drive select 1
29	30	O	Drive select 2
31	32	O	Drive select 3
33	34	O	Direction
35	36	O	Step pulse
37	38	O	Write data
39	40	O	Write gate
41	42	I	Track 00
43	44	I	Write protected
45	46	I	Read data, composite
47	48	-	Not used
49	50	O	Motor control

Figure 1a

For 5 1/4" Drives

Ground Pin #	Signal Pin #	Input - I Output -O	Description
1	2	O	Head load
3	4	-	Not used
5	6	I	Ready
7	8	I	Index
9	10	O	Drive select 0
11	12	O	Drive select 1
13	14	O	Drive select 2
15	16	O	Motor
17	18	O	Direction
19	20	O	Step
21	22	O	Write data
23	24	O	Write gate
25	26	I	Track 0
27	28	I	Write protected
29	30	I	Read data
31	32	O	Head 1
33	34	O	Drive select 3

Input/Output are referenced to FDC-II. Input is then a signal from the disk drive to FDC-II, and output is a signal to the disk drive.

Figure 1b

Options

Pre-Write Compensation

To help compensate for the shifting of data bits during the read operation of the floppy disk drive, the write data is shifted prior to the write operation. This is particularly critical for double-density operation. As seen in the previous disk drive section, different drives require different amounts of pre-write compensation. The symptoms of too much or not enough pre-write compensation are as follows: 1. Too much pre-write compensation shows up as read errors usually CRC) in the outer tracks (0-42); 2. Not enough pre-write compensation shows up as read errors in the inner tracks (43-76). Jumper pads are provided on the BACK of FDC-II to adjust the amount of compensation along with posts and shorting plug on the FRONT of FDC-II.

FRONT of FDC-II

34-pin connector

PW FD NC

BACK of FDC-II

8A

A1 PW1 B1 B2 PW2 A2

8B

Connection	Result
FD to PW	Standard. Provides Pre-Write Compensation
FD to NC	No Pre-Write Compensation
A1 to PW1 A2 to PW2	Standard. Provides 250 ns compensation for 8" drives, and 500 ns for 5 1/4" drives.
B1 to PW1 B2 to PW2	Provides 125 ns compensation for 8" drives, and 250 ns for 5 1/4" drives.

When both 5 1/4" and 8" drives are used in the same system, and the appropriate pre-write compensation for the 8" drive doesn't provide the correct 5 1/4" compensation, stay with the correct 8" compensation. Eight inch recording generally has more stringent requirements than the 5 1/4" recording.

Mini/Maxi Drive Selection

Access to either 5 1/4" or 8" drives is controlled by bit 4 of the status port (73H for the standard FDC-II). Output a 1 to select 5 1/4" drives, and a 0 to select 8" drives. Note that bit 7 of this port controls the boot PROM, and bit 2 controls the drive spindle motor. Thus when selecting 5 1/4" or 8" operation, the desired states of bits 2 and 7 must also be output.

```
LD  A,92H       ;This selects 5 1/4" drives, disables the boot
OUT (73H),A     ;PROM, and enables the spindle motor.

LD  A,82H       ;This selects 8" drives, disables the boot
OUT (73H),A     ;PROM, and enables the spindle motor.
```

Boot Drive Selection

On reset, the FDC-II boot program checks bit 1 of the status port to determine whether a 5 1/4" or 8" drive will be the source of the operating system. In the present software, if bit 1 is 0 (trace intact), an 8" drive is assumed. If bit 1 is 1 (trace cut), a 5 1/4" drive is assumed.

BACK of FDC-II

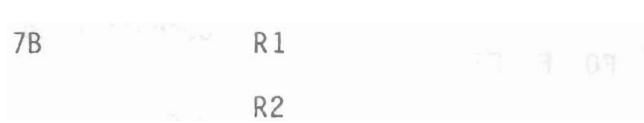
1. Cut trace to boot on 5 1/4" drive.

2. Trace intact, or solder a wire across the pads to boot from 8" drive.

Mini Drive READY Function

Some 5 1/4" floppy disk drives don't have a READY function. READY indicates to the controller that a diskette is properly inserted, the door is closed, and the spindle motor is running. The 765 waits for a READY indication before it will perform any operations on the drive. To accommodate those 5 1/4" drives without a READY function, the FDC-II has a circuit to activate the READY line when 5 1/4" drives are selected. For those 5 1/4" drives which have a READY function, this circuit should be disabled by cutting the trace between the two pads.

BACK of FDC-II



Cut the trace between R1 and R2 to disable the FDC-II automatic READY activation for 5 1/4" drives with that capability.

RAM Buffer Disable

For systems with a CPU that is fast enough to directly transfer data to the 765, the RAM buffer can be disabled. When the RAM is disabled, the FDC-II does not occupy any memory space. To disable the RAM buffer, cut the trace between the two pads.

BACK of FDC-II

M1

M2 RN

5F

Boot PROM Disable

The boot PROM is controlled by bit 7 of port 73H (Standard). On reset, this bit will be low, enabling the PROM and executing the load operation. If this function is to be handled elsewhere in the system, the boot function can be disabled by removing the plug. If this plug is removed the on-board PROM cannot be accessed by the system.

FRONT of FDC-II

2A 1A

2708/2758 Selection

The 2708 EPROM requires +5, -5, and +12 volts to operate. The 2758 requires only +5 volts. Jumpers on the back of FDC-II are installed according to the type EPROM used.

BACK of FDC-II

1E 2E

E0 E E1 F0 F F1

2708 (standard):
Connect E to E1
Connect F to F1

2758:
Connect E to E0
Connect F to F0

Extended Head Load

The uPD765 floppy disk controller has a maximum head unload time of 240 mSec. **In some applications this will cause an undue amount of head loading and unloading.** To increase this head unload time, and reduce the number of head load actions, a 74LS123 monostable can be wired into the head drive circuit. With the addition of a 6 volt capacitor and a resistor, the head unload time is extended. This increases the life of the media and the heads where there would normally be a great deal of head load activity. There is an empty socket for the 74LS123 in location 1A. The resistor and capacitor also have to be added. Using a 100 KOhms resistor gives the following table:

Capacitor (uF)	Head Load Time (sec)
10	0.5
30	1.4
50	2.3
70	3.2
90	4.1
110	5.0
130	5.9
150	6.8
170	7.7
190	8.6
210	9.5
230	10.4
250	11.3

The time values are approximate since normally resistor values are ± 10% and capacitor values ± 20%.

FRONT of FDC-II

Resistor

1A

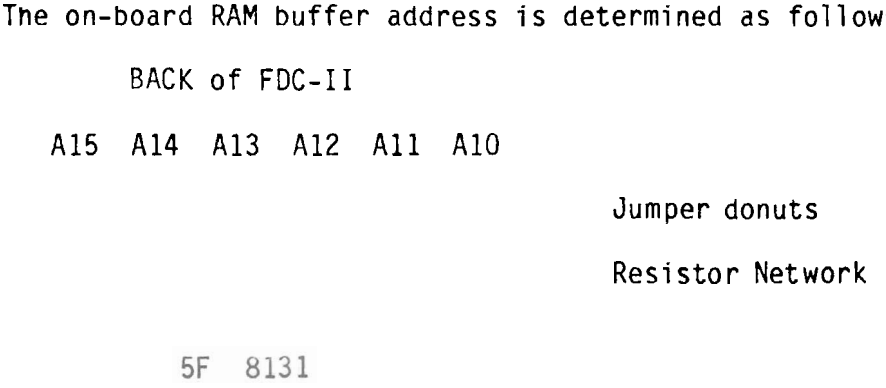
C C+ Capacitor

BACK of FDC-II

Cut trace between HL and NH. Jumper from HL to XH and from NH to TR.

Memory Addressing

The on-board RAM buffer address is determined as follows:



Standard address at F400H shown.

Upper Nibble (A15-A12):

Address	A15	A14	A13	A12	
F	1	1	1	1	Standard
E	1	1	1	0	
D	1	1	0	1	
C	1	1	0	0	
B	1	0	1	1	
A	1	0	1	0	
9	1	0	0	1	
8	1	0	0	0	

Lower Nibble (A11, A10):

Address	A11	A10	
C00	1	1	
800	1	0	
400	0	1	Standard
000	0	0	

Note: A "1" indicates no jumper; a "0" means jumper.

The complete address is formed from the upper and lower nibbles; thus an address with E as the upper nibble and 800 as the lower nibble is E800H. The RAM buffer occupies 1K of address space, so the standard address space is F400H to F7FFH.

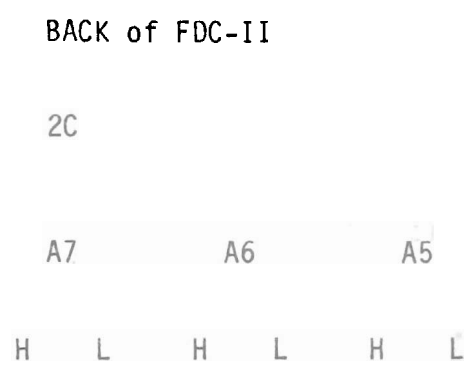
Note: The FDC-II from the factory has a trace on the solder side of the pc board. To change the address, this trace may need to be cut.

Caution: If the FDC-II buffer address is changed, the standard software in the boot PROM must be changed (if the boot is used), as must any operating system that accesses the FDC-II buffer.

I/O Addressing

The I/O address of FDC-II is determined as follows:

BACK of FDC-II



Address	A7	A6	A5	
E0-FF	H	H	H	L = connect L to address pad.
C0-DF	H	H	L	H = connect H to address pad.
A0-BF	H	L	H	
80-9F	H	L	L	
60-7F	L	H	H	Standard
40-5F	L	H	L	
20-3F	L	L	H	
00-1F	L	L	L	

Note: The FDC-II from the factory has traces on the solder side of the pc board which connect the standard address pads. These traces may need to be cut for different addressing.

Caution: Changing the FDC-II I/O address will require changes in the boot PROM (if used) and appropriate changes in any operating system that accesses the FDC-II ports.

I/O Port Assignments

The port assignments for the standard FDC-II are:

Port Address	Function
64H	DMA Control Channel 2
65H	DMA Channel 2 length
68H	DMA Control Mode
70H	FDC Status
71H	FDC Data
73H	Status, output ports

Note: The FDC-II occupies port addresses 60H through 7FH, though not all these ports are used currently.

Status/Output Port Bit Assignments

The status port is 73H in the standard board. This is an input port. Its bit assignments are:

Bit	Function
0	Free for user.
1	Used to select the boot drive size. If 0 then drive size is 8"; if 1 then drive size is 5 1/4".
2	Free for user.
3	Always at a logic high (1).
4	Always at a logic high (1).
5	Always at a logic high (1).
6	Always at a logic high (1).
7	Used to check the status of the FDC interrupt pin. If 1 then the FDC is interrupting otherwise it is not.

The output port is 73H in the standard board. Its bit assignments are:

Bit	Function
0	Not available.
1	Not available.
2	Used to control the motor on 5 1/4" or PerSci drives. A 0 means turn off the motor and a 1 turn on the motor.
3	Free for user.
4	Used to set the correct clock speed for the different drive sizes. For 8" drives should always be 0 and for 5 1/4" drives should always be 1.
5	Used to give a "Terminal Count" signal to the FDC chip. Output a 1 and then a 0 to generate the TC signal. Refer to the uPD765 manual for more details on the use of TC.
6	Free for user.
7	Used to select the on-board PROM. When 0 the PROM is selected and when 1 the PROM is deselected. Normally should always be 1 except during the bootstrap function.

Note: all the output bits are cleared (set to 0) upon RESET.

Theory of Operation

Refer to the parts layout and schematic for assistance in referencing the devices mentioned in the text.

I/O Addressing

The FDC I/O ports are selected by decoding the address lines A7, A6 and A5 of the S-100 bus. These three address lines and their complements are placed on pads adjacent to 2C. The input pins to 2C must be active high for an output active low to appear on pin 6. With the standard address of FDC-II, 60H to 7FH, this means that pin 4 of 2C connects to pin 2 of 3C and A-6 and A-5 connect directly to pins 2 and 1 of 2C respectively. Thus, when A-7 is low and A-6 and A-5 are high, 2C will be active if pin 5 is high, which occurs whenever the central processor in the system is executing an input or output instruction. SOUT is inverted by 1E and input to pin 10 of 2E. SINP is ANDed with PDBIN and this output, pin 3 of 2E, is fed to pin 9 of 2E. Thus, whenever SOUT is high or SINP and PDBIN are high, 2E pin 8 will be high, thus enabling the output from 2C which selects the FDC-II I/O ports.

The various chip select lines of the FDC-II, that is the DMA controller, the FDC and the FDC status line are generated by further decoding the address lines, specifically A-0, A-1 and A-4.

RAM Addressing

In the non-DMA mode, the FDC-II RAM address is selected by placing appropriate jumpers on the pins connecting to 5F, a 6-bit comparator. 5F is connected to the six high order address lines, AB-10 through AB-15. When the levels on those address lines match the levels selected by the jumpers, the output of 5F is low. This through the series of gates in 4A selects the RAM IC, 3B. The output of 5F is internally latched by a strobe signal at the enabling input on pin 7. This strobe is generated by inverting the PSYNC signal of the S-100 bus. If SINTA is active, or an I/O operation is in progress, the RAM will not be selected. In the DMA mode, 3B is selected by a combination of signals generated by 5C, the DMA controller. The address strobe from pin 8 of 5C is ORed with the inverted signal of AEN, and this signal is then fed into 1D to provide a low on the chip select line of 3B whenever there is an active DMA "read" or "write" operation. Note at this time that the "read" and "write" signals to 3B originate either from the S-100 bus or from the DMA controller, depending on the status of pin 9 of 5C, the AEN output. This is the address enable signal from the DMA controller and is high whenever the DMA controller is active. This signal is applied to the output enable pin of 2D, one half of an octal tri-state buffer. When AEN is active, the RAM "read-write" signals originate from the DMA controller. When AEN is inactive, that is, low, the "read-write" signals originate from the signals on the S-100 bus. The "write" signal for memory activity on the S-100 bus is an ANDing SOUT and PWR per the IEEE-100 specification. The "read" signal memory function is generated by ANDing PDBIN and SMEMR. This is the memory read status signal from the CPU and the processor data bus input mode (PDBIN) signal.

Data Bus Drivers

The data bus drivers of FDC-II are activated whenever the CPU accesses the FDC-II I/O ports or memory. The data-in bus driver, 3D, is enabled whenever PDBIN is active, 2C pin 8 is active high and AEN is low. These three signals are ANDed in 1C and the output, pin 12, enables 3D. 2C, pin 8, is active high whenever the FDC, DMA, BOOT PROM, or the RAM is active. The data-out bus driver which simply buffers the information output from the CPU into the FDC-II, is active whenever no DMA operation is occuring and PDBIN is inactive.

Boot Circuit

The on-board boot circuit is activated whenever reset on pin 75 of the S-100 bus is active low. This causes the clear line of 2A to be low causing pin 5 to be low. The phantom line is pulled low which turns off the output drivers of the system memory. Thus the processor sees the boot PROM and executes its program. However, the system memory can still receive information. The boot program loads itself into memory. When the move operation is finished, an output to port 73H sets bit 7 high which disables the boot PROM. The system memory will no longer be disabled by phantom, and the transferred boot program will be executed.

The program within the boot PROM turns on the drive spindle motor, then sets up the DMA controller and the floppy disk controller. Once it has accomplished that task, it then causes drive 0 to be recalibrated, that is to move its head to track 0 of the diskette. Then the boot routine reads in the first sector of track 0 and executes that routine which will be located at 0000H. The routine at 0000H will then read in the operating system from the appropriate tracks of the diskette and when the operating system has been loaded correctly, will execute it.

Read/Write Signals

The DMA control requires I/O read and write signals when in the slave mode and generates those signals when in the master mode. I/O read and write are generated by decoding the I/O input and output signals of the S-100 bus and combining those with the processor write signal, PWR, and the processor input signal, PDBIN. These read and write signals are then gated to the DMA and FDC via 2D whose outputs are active whenever no DMA operation is occurring.

DMA Controller

When the DMA controller is activated by command from the CPU, its address enable signal, AEN, goes high. AEN disable the address buffers, 4E and 4D. The high order address bits for the DMA operation are output on the data line at which time address strobe pin 8 is activated. This clocks the two high order address lines for the RAM chip into 5A, a latch. The low order address lines for 3B are presented on the address bus from the DMA controller. When the FDC has data to transfer, it signals the DMA controller on the DMA request line. The DMA controller acknowledges the DMA request and executes an I/O read or write as appropriate for the operation. The data is then output on the data bus

lines and written or read from the RAM. When the programmed block of information has been transferred, the DMA controller raises the terminal count line, pin 36, which then stops the FDC from transferring further information. At this point, the FDC will raise its interrupt line to signal to the CPU that the data operation has been completed.

Floppy Disk Controller

The FDC (Floppy Disk Controller), 5C, connects to the disk drives in the system. With handshaking signals, it controls the position of the read/write head and the flow of data to and from the diskette. 5B continuously monitors the status of all the drives in the system. It does this by time multiplexing the select lines 0 - 3 which in turn access drives 0 - 3. Whenever the status of a drive changes, that is when the ready line either goes active or inactive, 5B will signal the system via an interrupt on its status port. 5B selects drives via its unit select lines, pins 28 and 29, which are decoded by 7C, a dual 2-line to 4-line decoder. Operations of 5B occur either in a read/write mode or a seek mode. A seek mode is one in which a drive is physically moved to a particular track on the diskette. A read/write operation involves reading or writing information to a track of the diskette. 5B multiplexes several of its lines, depending on the function performed. This multiplexing is controlled by pin 39 of 5B and is inverted by 6B so that one-half of 6A is enabled during read/write operations and the other half is enabled during seek operations, thus the multiple function pins will be directed to the appropriate control lines of the disk drive depending on the operation being performed.

The data written to the diskette are compensated during the write operation. This is called pre-write compensation. This is done because under normal conditions, certain data patterns will be shifted slightly, reducing the margin for error in the read process. This shift is due to the magnetic recording process. 5B attempts to compensate for this shift through two outputs on pins 31 and 32 which are the preshift or precompensation outputs. The data from 5B on pin 30 is entered into a shift register, 8B, which is clocked by the same clock that operates 5B. 8A is a data selector which selects the appropriate bit time in the shift register according to the output from 5B. The output of 8A is then sent to the disk drive where it is recorded on the diskette.

Whenever 5B completes an operation, it raises its interrupt pin, pin 18, and waits for the system to interrogate it to determine what the status of the operation is. The CPU addresses the FDC status port of the FDC-II which activates 2D which then sends the interrupt signal onto the data bus through data input bit 7. The CPU will then execute appropriate operations to determine why the interrupt line is active and to sense the status of the FDC.

Note that all the lines from the floppy disk drive are terminated in resistor network 2 which is composed of a resistor divider where one-half of the divider is connected to ground through a 330 ohm resistor and the other half connected to +5 volts through a 220 ohm resistor. This combination provides a passive pull-up for the drive signals and terminates the ribbon cable in an impedence which closely approximates the impedence of the cable. This resistive termination of the cable

helps improve the rejection of electrical noise and interference and improves the integrity of the data received from the floppy disk drive.

Software Interface

This section will discuss the overall set-up and operational requirements of the DMA and FDC IC's. Only an overview of the device requirements will be presented due to the number and types of operations of which these devices are capable.

DMA IC Set-up

The DMA IC must be initialized as follows: it must be told the address of the on-board data buffer, which is 0000 to the DMA IC. Then the number of bytes to transfer and the data direction (to or from the disk drive) must be specified. When ready to read, the DMA IC must be activated. The sequence of commands would be (for the standard FDC-II):

Output 00H to port 64H

Output 00H to port 64H (must be done twice)

Output 7FH (128 bytes) or FFH (256 bytes) for number of bytes to transfer to port 65H

Output 80H (write to drive) or 40H (read from drive) for data direction to port 65H.

When ready to transfer data, output 44H to port 68H, which turns the DMA channel on.

Note: For multiple-sector read operations, the lower nibble of the data direction byte will be non-zero. See the Intel data sheet for further information on the capabilities of the 8257.

FDC IC Set-up

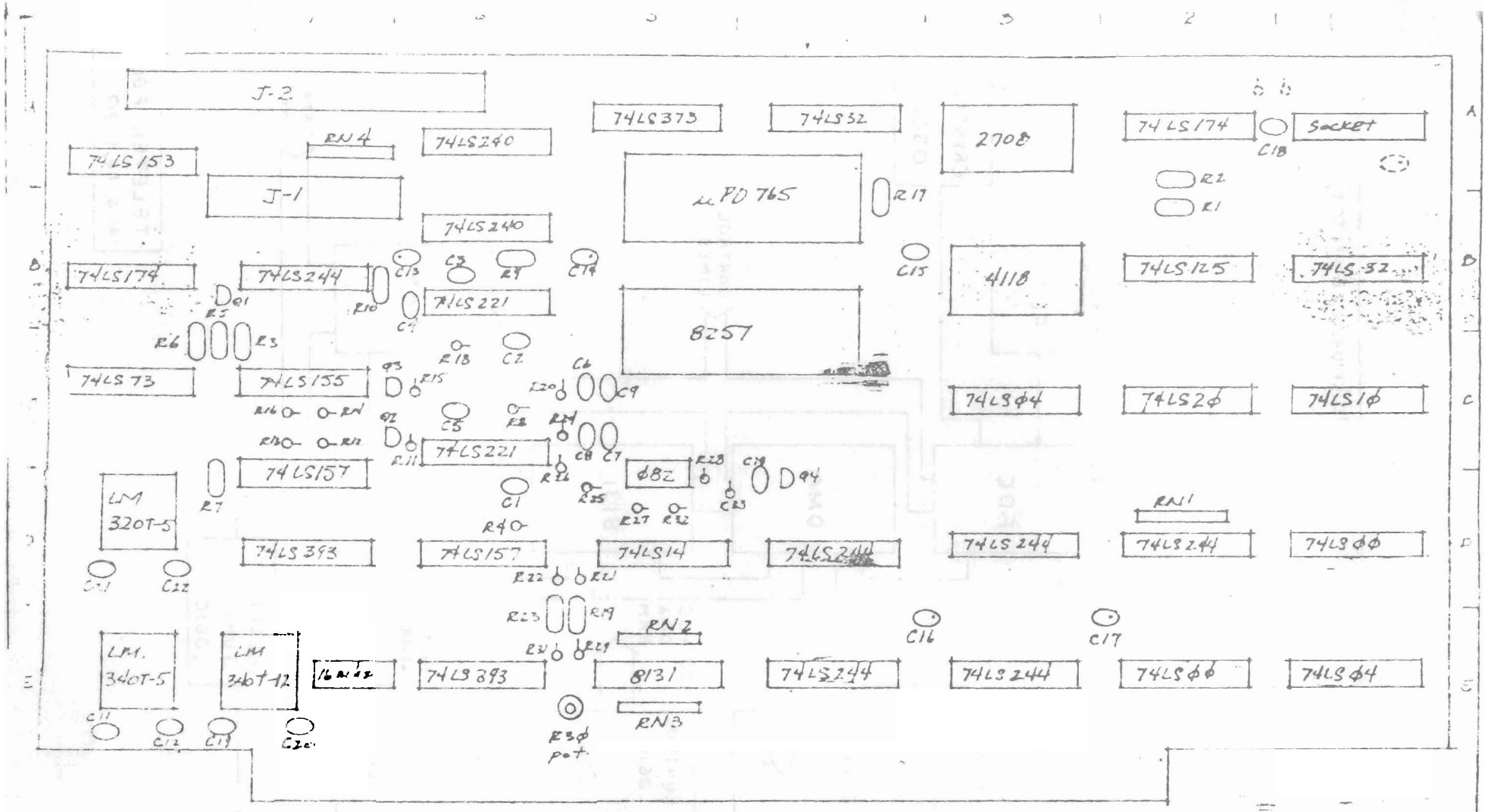
The following discussion will cover the general requirements of the NEC 765. For detailed information of the complexities and sophistication of the 765, consult the NEC manual.

Before sending any information to the 765, the status of the RQM (Request for Master) bit must be checked. When it is high, a control byte may be sent to the Data Register, port 71H. The RQM is bit 7 of port 70H, the status port.

The 765 FDC must be set up with the attributes desired for the flexible disk drive used. These attributes are: Step Rate Timing (SRT) which is the time required by the drive to step from one track to the next; Head Unload Timing (HUT) which is the time the head stays loaded against the diskette after the last read or write operation; Head Load Timing (HLT),

the time required for the head to settle down after being loaded; and last, set the 765 in its DMA mode. These attributes are loaded using the "SPECIFY" command of the 765.

Whenever the 765 completes an operation that generates an interrupt, such as a read or write, bit 7 of port 73H will be high. When this bit is high, the RQM bit must be checked until it goes high, then the DIO (Data Input/Output) bit checked. If DIO is high, data must be read from the data register until the Status Register indicates RQM high and DIO low. After each Seek and Recalibrate command, a Sense Interrupt Status command must be sent to determine the status of the drives and to terminate the Interrupt request.

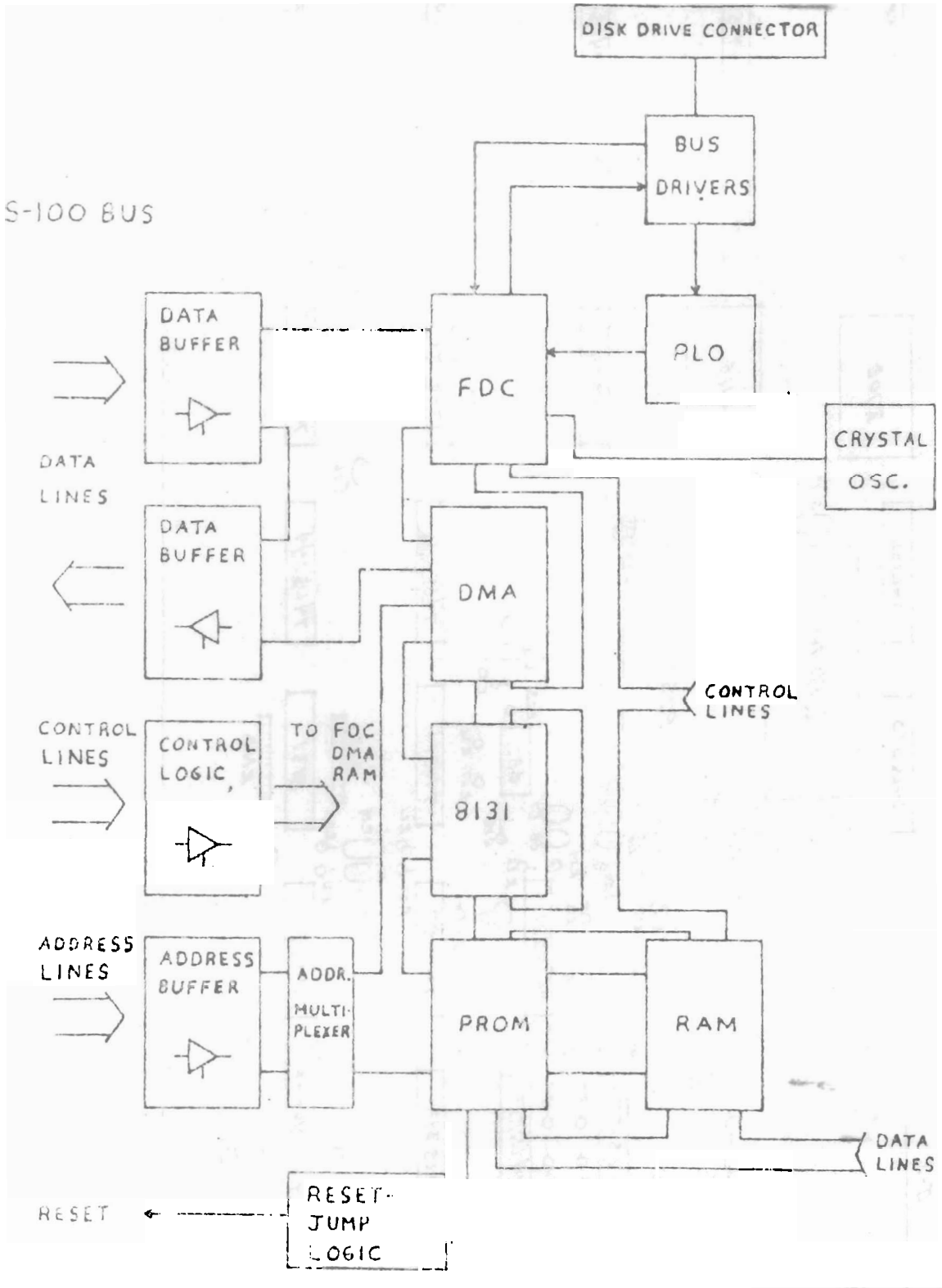


FDC-II User Manual, Appendix A

TELETEK FDC-II BOARD LAYOUT

FDC-II User Manual, Appendix B

BLOCK DIAGRAM FDC-II



TELETEK FDC-II
AUG. 18, 1980

Contents

Disk Drive Interfacing

In controlling a disk drive from FDC-II, proper connections must be made to the disk drive in order for it to be operational. The drive options must be configured as outlined in the appropriate manufacturer's section following this introduction. Particularly important is the fact that the uPD-765 continuously polls all drives in the system to keep track of their status. With some drives this will interfere with their seek function (positioning of the head). Thus, most drives will have a stepper motor enable option, or simultanious seek option, that powers the stepper motor continuously, rather than just when the drive is selected. If the drive won't read initially, check for this option.

Drive interfacing deals with the proper connection of functional signals and the satisfying of electrical and mechanical requirements.

To help ease the shock of transition from the interchanging of various disk drives to other host controllers, a standard known as ANSI was developed which standardized the means of intercommunication between disk drive and host controller by specifying power requirements and voltage levels, edge connector and cable specifications, and specific pin numbers of the connector to particular functional signals.

ANSI Standards

Functional signals assigned to specific pin numbers of the connector are shown below for a 5.25-inch disk drive and an 8-inch disk drive.

ANSI Standard for 5.25 Inch Drive

Signal Pin No.	Ground Pin No.	Signal
2	1	Not assigned (Head load)
4	3	In use control
6	5	Drive select 3 (Ready)
8	7	Index/sector
10	9	Drive select 0
12	11	Drive select 1
14	13	Drive select 2
16	15	Motor on
18	17	Direction select
20	19	Step
22	21	Composite write data
24	23	Write gate
26	25	Track 0
28	27	Write protected
30	29	Composite read data
32	31	Side one select
34	33	Disk change (Drive select 3)

ANSI Standard for 8-Inch Drive

Signal Pin No.	Ground Pin No.	Signal
2	1	Head current switch
4	3	Not assigned
6	5	Not assigned
8	7	Drive busy
10	9	Two-sided
12	11	Disk change
14	13	Side one select
16	15	In use control
18	17	Head load
20	19	Index
22	21	Drive ready
24	23	Sector
26	25	Drive select 0
28	27	Drive select 1
30	29	Drive select 2
32	31	Drive select 3
34	33	Direction select
36	35	Step
38	37	Composite write data
40	39	Write gate
42	41	Track 0
44	43	Write protected
46	45	Composite read data
48	47	Separated read data
50	49	Separated read clock

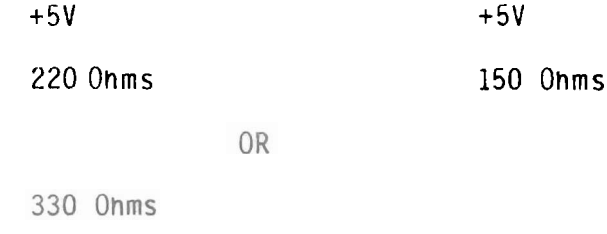
Electrical

1. Multi Drop Bus: Multiple drives may be connected to the same host controller as shown in Figure 1. Only one drive is logically connected to the interface at a time.

2. Voltage Levels (as measured at the driver)

Logical true	Active low	+0V to +0.4V
Logical false	Active high	+2.4V to +5.5V

3. Termination: Signal lines shall be terminated by one of the two resistive networks illustrated below, whether the termination occurs at the drive or the host, but only at the terminal point of a signal.



4. Signal Drivers: The signal drivers should have open collector output stages capable of sinking a minimum of 40mA at logical true (low) level, with maximum voltage of 0.4V as measured at the driver output.

5. Signal Receivers: The signal receivers should not unduly load the multi drop bus and should not require more than 40uA current from the driver at input high (2.4V) nor supply more than 1.6mA to a current sink at input low (0.4V) level.

Interconnecting Cable

Conductor Size

Copper
AWG #30 or larger for solid conductor
AWG #28 or larger for stranded conductor

Non-copper
Sufficient size as to yield a dc resistance not to exceed 110 Ohms per 1000 ft. per conductor.

Stray capacitance
Capacitance between one wire in a cable and all others in the cable with all others connected to ground shall not exceed 40pF/ft. and the value shall be reasonably uniform over the length of the cable.

Mutual pair capacitance
Capacitance between one wire of the pair to the other shall not exceed 20pF/ft. and the value should be reasonably uniform over the length of the cable.

Micropolis 1015 Disk Drive

Required drive configuration:

1.	DS1-4	Select appropiate drive address
2.	HDLD	Enable this option

Install the termination network only in the last drive in the daisy chain.

Each drive requires 12 volts at 1.3A and 5 volts at 0.5A.

Required Pre-write Compensation: 250 ns.

Shugart SA-400 Disk Drive

Required drive configuration:

1.	HL	Jumper
2.	DS-1,2,3	Select appropiate drive address
3.	MX	Open
4.	MH	Open

Install the termination network only in the last drive in the daisy chain.

Each drive requires 12 volts at 1.8A and 5 volts at 0.7A.

Required Pre-write Compensation: none. (If pre-write compensation is wanted use 250 ns.)

MPI B-51/52 Disk Drive

Required drive configuration:

1. T1	Jumper
2. T2-T4	Select appropiate drive address
3. T5	Open
4. T6	Open
5. T7	Open

Install the termination network only in the last drive in the daisy chain.

Each drive requires 12 volts at 1.5A and 5 volts at 0.7A.

Required Pre-write Compensation: none.

Note: The FDC-II does not provide Drive Select 3 on pin 6 of the 34 pin connector. Thus this line must be disconnected going into the drive.

Caldisk 143M Disk Drive

Required drive configuration:

1.	DS A	Closed (DS = Dip Switch)
2.	DS B	Open
3.	DS C	Open
4.	DS D	Open
5.	JPR1	Open
6.	JPR2	Open
7.	JPR3	Open
8.	JPR4	Jumper
9.	JPR5	Open
10.	JPR6	Open
11.	JPR7	Jumper
12.	JPR8-11	Select appropiate drive address
13.	JPR12	Jumper
14.	JPR13	Open
15.	JPR14	Open
16.	JPR15	Open
17.	JPR16	Open

Install the termination network only in the last drive in the daisy chain..

Each drive requires 24 volts at 1.5A and 5 volts at 1.0A.

Required Pre-write Compensation: none.

Innotronics 410/420 Disk Drive

Required drive configuration*:

1. EH	Trace intact
2. AH	Open
3. TH	Trace intact
4. NT	Open
5. TE	Trace intact
6. NT	Open
7. LM	Trace intact
8. TM	Open
9. WP	Trace intact (2 places)
10. NP	Open (2 places)
11. T4	Jumper
12. T3, T5, T7	Jumpered on last drive in system
13. SO-3	Select appropriate drive address

To use the Model 420 (Hard Sector) Disk Drive as a Soft Sector Disk Drive, the following link positions must be set:

1. IB	Jumper
2. HS	Open
3. RD	Jumper
4. SD	Open (2 places)
5. VV	Jumper to accept -5 volt supply, otherwise open to accept -7 to -12 volts.

Install the termination network only in the last drive in the daisy chain.

Each drive requires +5 volts at 0.8A, -5 volts at .08A, and +24 volts. The current rating for the 24 volts supply depends on whether the drives will seek individually or simultaneously. If CP/M or a similar DOS is used, the total current is 1.4A. This is because Innotronics applies power to the stepper motor only when the drive is seeking. If software is used that can simultaneously seek on all drives in the system, each individual drive will require 1.4A.

Required Pre-write Compensation: 125 ns.

*The model 410 disk drives are shipped fully compatible with the FDC-II.

PerSci 277 Disk Drive System

The PerSci 277 disk drive system is a system composed of two 8-inch drive units requiring a 50 pin connector to the host system used. Pin assignments to functional signals of the 50 pin connector and the changes required to interface to FDC-II are shown below.

FDC-II	Signal Pin No.	Ground Pin No.	Signal
2	2	1	Unassigned
4	4	3	Drive select 2 right
6	6	5	Ready 1
Cut	8	7	Index 1
Cut	10	9	Seek complete
12	12	11	Restore
Cut	14	13	Remote eject 0
18	16	15	Direct headload
Cut	18	17	Drive select 2 left
20	20	19	Index 0
22	22	21	Ready 0
50	24	23	Spindle motor enable
26	26	25	Drive select 1 left
28	28	27	Drive select 1 right
Cut	30	29	Write protect 1
Cut	32	31	Remote eject 1
34	34	33	Direction select
36	36	35	Step
38	38	37	Write data
40	40	39	Write gate
42	42	41	Track 0
44	44	43	Write protect 0
46	46	45	Read data
48	48	47	Separated data
Cut	50	49	Separated clock

Required drive configuration:

1. Address DIP, U-11: connect pin 4 to 11, and pin 2 to 13.
2. A-B — Raw read data
3. D-BL — Select gate enabled
4. E,F,G — Open
5. J-Z — Enable L=0, and R=1
6. K-L — Wire-OR the Write Protect signals
7. M,N,P — Open
8. R,S,T — Open
9. U-V — Wire-OR the Index signals
10. W-X — Enable Index 0
11. AB-AC — Enable Index 0
12. AD-AE — Enable Index 1
13. AH-AJ — Enable Index 1
14. AM-AL — For spindle motor control
    or
    AM-AN — Spindle motor runs continuously

Innotronics 410/420 Disk Drive

Required drive configuration*:

1. EH	Trace intact
2. AH	Open
3. TH	Trace intact
4. NT	Open
5. TE	Trace intact
6. NT	Open
7. LM	Trace intact
8. TM	Open
9. WP	Trace intact (2 places)
10. NP	Open (2 places)
11. T4	Jumper
12. T3, T5, T7	Jumpered on last drive in system
13. SO-3	Select appropriate drive address

To use the Model 420 (Hard Sector) Disk Drive as a Soft Sector Disk Drive, the following link positions must be set:

1. IB	Jumper
2. HS	Open
3. RD	Jumper
4. SD	Open (2 places)
5. VV	Jumper to accept -5 volt supply, otherwise open to accept -7 to -12 volts.

Install the termination network only in the last drive in the daisy chain.

Each drive requires +5 volts at 0.8A, -5 volts at .08A, and +24 volts. The current rating for the 24 volts supply depends on whether the drives will seek individually or simultaneously. If CP/M or a similar DOS is used, the total current is 1.4A. This is because Innotronics applies power to the stepper motor only when the drive is seeking. If software is used that can simultaneously seek on all drives in the system, each individual drive will require 1.4A.

Required Pre-write Compensation: 125 ns.

*The model 410 disk drives are shipped fully compatible with the FDC-II.

15.	AP-AR	Wire-OR the Ready signals
16.	AS-AT	Remote eject, connects L and R together
17.	AU,AV,AW	Open
18.	BA-BB	Enable Index 1
19.	BD-BE	Seek complete enable
20.	BF,BH,BJ	Open
21.	BK-BM	Enable Index 0

Each drive requires 24 volts at 1.3A, 5 volts at 2.2A, -5 volts at 0.2A and for the spindle power, 7 - 10 volts 2.0A.

Because the PerSci has two physical drives connected to one head positioner, the software must be made to seek and recalibrate only drive 0. Otherwise the uPD-765 will seek on both drives 0 and 1, and position past the correct track.

If fast seek is required (seek rate less than the standard 10 ms step), the seek complete line must be connected to an unused pin of IC 2D, and a 150 ohm 1/4 watt resistor connected to +5 volts. Contact the factory for further information relating to software requirements.

Add 150 ohm resistor
for fast seek.

2A

Required Pre-write Compensation: 250 ns.

Qume DT-8 Disk Drive

Required drive configuration:

1. A	Jumper
2. B	Open
3. X	Jumper
4. Z	Jumper
5. HL	Open
6. R	Jumper
7. I	Jumper
8. RI	Trace intact
9. RR	Trace intact
10. C	Jumper
11. D	Open
12. DC	Open
13. 2S	Open (Jumper for double sided)
14. DS	Open
15. Y	Open
16. DL	Open
17. WP	Trace intact
18. NP	Open
19. S2	Trace intact
20. S1, S3	Open
21. DS1-4	Select appropriate drive address
22. B1, 2, 3, 4	Open

Install 2 resistor terminator modules into the last drive in the daisy chain.

Each drive requires 24 volts at 0.9A and 5 volts at 1.1A.

Required Pre-write Compensation: none.

Shugart 800/801 Disk Drive

Required drive configuration:

1.	X	Jumper
2.	DC	Open
3.	D	Open
4.	C	Jumper
5.	I	Trace intact
6.	R	Trace intact
7.	S	Trace intact
8.	DS1-4	Select appropriate drive address
9.	T1, 3, 4, 5, 6	Jumper on last drive in system
10.	T2	Jumper
11.	HL	Open
12.	DS	Open
13.	RI	Trace intact
14.	RR	Trace intact
15.	Y	Open
16.	Z	Jumper
17.	800	Jumper
18.	801	Open
19.	A	Jumper
20.	B	Open

Each drive requires 24 volts at 1.7A, +5 volts at 1.0A, and -5 volts at 0.07A. Note: Many power supplies for floppy drives do not have the required current capability for 2 or more Shugart drives.

Required Pre-write compensation: 250 ns.

Siemens FDD 100-8D Disk Drive

Required drive configuration:

1.	RAD SEL 0-3	Select appropriate drive address
2.	RAD STEP	Jumper pads labelled "2"
3.	"36"	Jumper
4.	A	Open
5.	"34"	Jumper
6.	B	Open
7.	RR	Jumper
8.	"22"	Jumper
9.	RI	Jumper
10.	C	Open
11.	"20"	Jumper
12.	"24"	Jumper
13.	L	Jumper
14.	J	Open
15.	K	Open
16.	"18"	Jumper
17.	M	Open
18.	SS	Jumper
19.	HS	Open
20.	S	Jumper
21.	U	Jumper
22.	R	Open
23.	H	Open (for Activity Indicator)
24.	"16"	Open
25.	E	Jumper
26.	V	Open
27.	"12"	Jumper
28.	G	Open (cut trace)
29.	H	Open (for Phase Option)
30.	F	Jumper

Install the terminator resistor pack in the last drive of the daisy chain.

Each drive requires 24 volts at 1.6A, and +5 volts at 1.0A.

The Siemens drives need to be modified if more than 1 drive will be in the system. On the drive p.c. board, locate IC 4D, a 7402. Cut trace coming from pin 4. Next, locate IC 4E (normally there should not be an IC in this location). Install a jumper wire from pin 12 of IC 4E to the "RI" pads on the p.c. board. This change accommodates the NEC controller.

Required Pre-write Compensation: 250 ns.

Remex 2000/4000 Disk Drive

Required drive configuration:

1.	2S	Jumper
2.	DC	Open
3.	C	Jumper
4.	D	Open
5.	DS1-4	Select appropriate drive address
6.	1B, 2B, 3B, 4B	Open
7.	S1, 2, 3	S2
8.	TS-FS	Don't care
9.	4000/4001	4000
10.	DL	Jumper
11.	S	Jumper
12.	R	Jumper
13.	I	Jumper
14.	X	Jumper
15.	B	Open
16.	A	Jumper
17.	HL	Open
18.	Z	Jumper
19.	DS	Open
20.	Y	Open
21.	RI	Traces intact
22.	RR	Traces intact

The last drive in the daisy chain must have the resistor termination pack installed in location 7A.

Each drive requires 24 volts at 0.6A, +5 volts at 1.0A, and -5 volts at 0.05A.

Required Pre-write Compensation: 250 ns.

MFE 500/700 Disk Drive

Required drive configuration:

1.	SE1,SE2	Open
2.	SE3	Open
3.	L-1	Jumper
4.	L-2	Open
5.	L-3	Open
6.	DL-0	Don't care
7.	DS-1 thru DS-4	Select appropiate drive address
8.	HL3, HL5	Open
9.	HL1, HL2, HL4	Jumper
10.	RR	Jumper
11.	RIS	Jumper
12.	J-4	Jumper
13.	J-6	Jumper
14.	J-7	Jumper
15.	DL0, DL1	Trace intact
16.	DL2, DL3	Open
17.	PRU	Trace intact
18.	PRL	Open
19.	J-5	Jumper
20.	LC2, PS6	Jumper
21.	PS2, LC6	Open
22.	SS1, SS2	Jumper
23.	SS3, SS4	Open
24.	WP1	Jumper
25.	WP2	Open

Only the last drive in the daisy chain should have the termination circuit (Z-15) installed.

Each drive requires 24 volts at 1.4A, +5 volts at 1.2A, and -5 volts at 0.025A.

Required Pre-write Compensation: 250 ns.

FDC-II Application Note

Subject: Seattle Computer Products 8086 CPU Board

Due to the timing requirements of the uPD765 and the 8257 it is not possible to run the FDC-II at 8 MHz without adding a wait state to all I/O operations on the FDC-II. The FDC-II has a wait state generator that is normally used for the on board bootstrap EPROM. If the bootstrap EPROM is not used it is possible to use this wait state generator for FDC-II I/O operations. This requires the following modification: cut the trace going to pin 9 of IC 6D. Put a jumper between pin 9 of IC 6D and pin 5 of IC 2C. This will add a wait state on any I/O operation on the FDC-II.